Remarks/Arguments:

Claims 1-22 are presently pending. Claims 1-6, 8-12, 14-18, 21, and 22 stand rejected and claims 7, 13, 19, and 20 are objected to but have been identified as allowable if rewritten in independent form. Applicant herein amends claims 1, 9, 15, 17, and 21. Support for the claim amendments can be found throughout the specification as originally filed. For example, see Figure 2 and paragraphs 29 and 34. Applicant contends that no new matter is added. Applicant respectfully requests reconsideration in view of the above amendments and following remarks.

Section 6 of the Office Action recites that "Claims 1-6, 8-12, 14-18, 21-22 are rejected under 35 U.S.C. 103(a) as being unpatenable over Nystuen (2004/0088472) in view of Shiozaki et al. (4,683,533)." Claim 1 includes at least one feature that is not disclosed, taught or suggested by Nystuen in view of Shiozaki. Claim 1 is directed to a memory controller and includes the following features (at least one of which is not found in the applied references):

> an arbiter having a plurality of request ports, each request port configured to receive the memory requests from a respective one of the plurality of requesters, the arbiter assigning a first memory request to a first processing path and a second memory request to a second processing path responsive to the memory banks requested by the received and assigned memory requests;
>
> a first path controller coupled to the arbiter and the plurality of memory banks, the first path controller configured to process the first memory request in the first processing path to activate a first memory bank associated with the first memory request for a first data transfer;
>
> a second path controller coupled to the arbiter and the plurality of memory banks, the second path controller configured to process the second memory request in the second processing path to activate, during the first data transfer, a second memory bank associated with the second memory request for a second data transfer; and
>
> a synchronizer coupled between the first path controller and the second path controller for synchronizing the first and second path controllers such that the first and second memory requests processed by the first and second path controllers, respectively, and the first and second data transfers do not conflict.

This means that an arbiter has a plurality of request ports for receiving memory requests from prospective requesters. The arbiter assigns the requests from the requesters to a first processing path and a second processing path. A first path controller processes the first memory request to activate a first memory bank for a first data transfer and a second path controller processes the second memory request to activate during the first data transfer and a second memory request for a second data transfer. A synchronizer coupled between the first path controller and the second path controller synchronizes the first and second path controllers so that the memory requests and the resultant data transfers do not conflict.

Nystuen is directed to a multi-mode memory controller. The memory controller includes a request input for receiving successive memory access requests and a memory interface configured for coupling to a memory device having a plurality of banks. See Abstract of Nystuen.

Shiozaki is directed to a storage control system using plural buffer address arrays. The storage control system controls the update operations on two buffer address arrays and a data processing system in which a plurality of processors are connected to a shared storage. See Abstract of Shiozaki. The background of Shiozaki describes a conflict situation in a multi-processor system including processors having buffer storages which share a main storage. In these systems, if a processor updates a data item stored at a given address in the main storage and if the data item stored at the given address has been retained in a buffer storage of another processor, there will be a conflict between the data items on the buffer and main storages. Techniques are then described for handling this cache coherency problem. A stated objective of Shiozaki is to provide a storage control system which avoids an invalid operation due to a temporary data inconsistency between the buffer storage and the shared storage associated with the update operation conducted. See Summary of Shiozaki. Thus, the conflicts addressed in Shiozaki appear to be data inconsistencies between multiple storage devices.

Nystuen and Shiozaki, however, fail to disclose, teach or suggest an arbiter that has a plurality of request ports where each request ports receives memory requests from a respective one of a plurality of requesters and the arbiter that assigns memory requests to first and second processing paths. As set forth above, Nystuen deals with successive memory requests and, thus, does not include an arbiter with multiple ports for receiving requests from respective requesters and assigning these requests to first and second processing paths as called for by claim 1. Shiozaki also fails to disclose such an arbiter.

Nystuen and Shiozaki further fail to disclose a synchronizer coupled between first and second path controllers for synchronizing the first and second path controllers such that first and second memory requests and first and second data transfers do not conflict as set forth above.

Section 6 of the Office Action recites that "Nystuen discloses ... a synchronizer coupled between the first path controller and the second path controller for synchronizing the first and second path controllers such that the first and second memory requests processed by the first and second path controllers, respectively, do not conflict [col. 1, ll 33-38; col. 2, ll 17-23 and col. 3, ll 25-36]." The cited locations in this section, however, appear to refer to Shiozaki rather than Nystuen. For example, the citations for the synchronizer portion of the paragraph refer to column and line numbers as found in the Shiozaki patent, whereas the remainder of the citations in that paragraph reference paragraph numbers as found in the Nystuen patent application publication. Accordingly, applicant will address this statement with respect to Shiozaki. As set forth above, Shiozaki is concerned with updating multiple memory locations in order to avoid data inconsistencies between buffer storage and main storage (i.e., cache coherency). Claim 1, however, is directed to synchronizing memory requests such that those memory requests and their associated data transfers do not conflict. Accordingly, Shiozaki does not teach a synchronizer as set forth in claim 1. Nystuen is likewise devoid of such a synchronizer.

Further, it would not have been obvious to combine the synchronizer of Shiozaki with the multimode memory controller of Nystuen. Nystuen is directed to managing successive memory access requests to a bank of memories. The synchronizer in Shiozaki, however, is directed to avoiding data inconsistencies between a buffer storage and a shared storage. The problem addressed with the synchronizer in Shiozaki is not applicable to the management of the successive memory requests in Nystuen. Accordingly, it would not have been obvious to combine this synchronizer of Shiozaki with the system of Nystuen.

Thus, the applied references (either alone or in combination) fail to disclose, teach, or suggest at least two features of claim 1. Accordingly, applicant respectfully requests that the rejection of claim 1 be withdrawn.

Claims 9 and 15, while not identical to claim 1, include features similar to claim 1. Accordingly, applicant contends that claims 9 and 15 are also allowable over the applied references for at least the reasons set forth above.

Claim 17 includes at least one feature that is not disclosed, taught, or suggested by Nystuen and Shiozaki. Claim 17, as amended, is directed to an arbitration method for assigning at least one controller to manage a plurality of memory requests from a plurality of requesters to a memory device having at least one memory bank. Claim 17, as amended, includes the following features:

> receiving at a plurality of requests ports the plurality of memory requests from the plurality of memory requesters during a current arbitration cycle, each request port configured to receive the memory request from a respective one of the plurality of requesters;
>
> comparing the plurality of memory requesters to a grant history register to identify ones of the plurality of memory requesters that have not had previous memory requests granted during the current arbitration cycle;
>
> assigning a memory request to one of the at least one controllers from one of the identified plurality of memory requesters have not had previous memory requests granted during the current arbitration cycle using fixed priority logic; and
>
> adding the requester of the assigned memory request to the grant history register.

This means that the arbiter looks at a grant history register to determine if a requester has accessed a memory bank during a current arbitration cycle and if that requester has not accessed the memory request, the arbiter may assign the memory request from that requester.

Nystuen fails to disclose, teach, or suggest at least the step of "assigning a memory request to one of the at least one controllers from one of the identified plurality of memory requesters that have not had previous memory requests granted during the current arbitration cycle using fixed priority logic." Nystuen does disclose a history register, i.e., history register 512. The history register in Nystuen, however, is used to determine when to precharge a memory bank rather than for purposes of assigning memory requests as called for in claim 1. Thus, Nystuen fails to disclose, teach, or suggest assigning a memory request to one of at least

one controller from the plurality of memory requesters not in the grant history register using fixed priority logic. Likewise, Shiozaki fails to disclose, teach, or suggest this feature. Accordingly, applicant contends that claim 17 is allowable over the applied references and respectfully requests that the rejection of claim 17 be withdrawn.

Claim 21, while not identical to claim 17, includes features similar to claim 17. Accordingly, applicant contends that claim 21 is also allowable over the applied references for at least the reasons set forth above.

Claims 2-6, 8, 10-12, 14, 16, 18, and 22 include all of the features of the independent claim from which they ultimately depend. Thus, claims 2-6, 8, 10-12, 14, 16, 18, and 22 are also allowable over the cited references for at least the reasons set forth above with respect to independent claims 1, 9, 15, 17, and 21. Accordingly, applicant contends that claims 2-6, 8, 10-12, 14, 16, 18, and 22 are likewise allowable and, therefore, respectfully requests that the rejection of these claims be withdrawn.

Applicant acknowledges with appreciation the Examiner's finding that dependent claims 7, 13, 19, and 20 include allowable subject matter and would be allowed if rewritten in independent form. Applicant submits, however, that there is no need to rewrite these claims in order to place them in condition for allowance because these claims are either directly or indirectly dependent on one of claims 1, 9, and 17, which for the reasons discussed above are also in condition for allowance.

In view of the amendments and remarks set forth above, applicant respectfully submits that claims 1-22 are in condition for allowance and early notification to that effect is earnestly solicited.

Respectfully submitted,

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The Director is hereby authorized to charge or credit Deposit Account No. **18-0350** for any additional fees, or any underpayment or credit for overpayment in connection herewith.

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Kathleen P. Carney